REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed December 17, 2004. Upon entry of the amendments in this response, claims 1 – 24 and 34 remain pending, claims 25 – 33 having been withdrawn. In particular, Applicant has amended claims 1, 3 – 16 and 21 – 24, and has added claim 34. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

In the Specification

The Office Action indicates that the title is not descriptive of the invention. As set forth above, Applicant has amended the title and respectfully asserts that the amended title is indicative of the invention to which the claims are directed.

Claim Objections

The Office Action indicates that the claims are objected to due to various informalities. As set forth above, Applicant has amended the claims and respectfully asserts that the objections have been accommodated.

Rejections under 35 U.S.C. 102

The Office Action indicates that claims 16 and 21 - 24 are rejected under 35 U.S.C 102(b) as being anticipated by *Lee* (U.S. 6,249,414) (hereinafter "*Lee* '414"); that claims 1 and 6 - 15 are rejected under 35 U.S.C 102(b) as being anticipated by *Lee* (U.S. 6,271,999) (hereinafter "*Lee* '999"); that claims 16 - 18 and 20 are rejected under 35 U.S.C 102(b) as being anticipated

by *Watanabe* (U.S. 3,806,773); and that claims 16, 18 and 19 are rejected under 35 U.S.C 102(b) as being anticipated by *Ito* (U.S. 5,604,655). Applicant respectfully traverses the rejections.

In this regard, claim 1 has been amended to recite:

> 1. A power-to-power semiconductor ESD protection structure on a semiconductor substrate comprising:
> at least one first doped regions within said substrate having opposite dopant than said substrate;
> a second doped region within each said first doped region having opposite dopant type than each said first doped region;
> at least one third doped regions within said substrate having opposite dopant type from said substrate, each said third doped region forming a doped pair with each said second doped region;
> conductor elements connecting said third doped region of one said doped pair to said second doped region of a subsequent said doped pair;
> a conductor element from said second doped region of a first said doped pair to a first voltage source; and
> a conductor element from said third doped region of a last said doped pair to a second voltage source;
> ***wherein each said first doped region is substantially free of doped regions having the same dopant type.***

(*Emphasis Added*).

Applicant respectfully asserts that *Lee* '999 is legally deficient for the purpose of anticipating claim 1. Specifically, Applicant respectfully asserts that this reference does not teach or otherwise disclose at least the features/limitations emphasized above in claim 1.

In this regard, *Lee* '999 does not teach or suggest "wherein the first doped region is substantially free of doped regions having the same dopant type." In particular, *Lee* '999 discloses a clamping diode ESD protection circuit, wherein N+ contacts 310a~310m are diffused to a highly doped concentration into the N-wells 305a~305m. See figure 3 and column 3 lines 33-35 of *Lee* '999. Therefore, Applicant respectfully asserts that the rejection of claim 1 under *Lee* '999 is improper and requests that the rejection be removed.

Since claims 6 - 15 and 34 are dependent claims that incorporate the limitations of claim 1, and are not otherwise rejected in the Office Action, Applicant respectfully asserts that claims 1, 6 - 15 and 34 are in condition for allowance. Additionally, claims 6 – 15 and 34 recite other limitations that can serve as an independent basis for patentability.

With respect to claim 16, that claim has been amended to recite:

> 16. A power-to-power semiconductor ESD protection structure on a semiconductor substrate comprising:
>
> a first doped region within said substrate having opposite dopant than said substrate;
>
> ***only one a second doped region within said first doped region having opposite dopant type to said first doped region***;
>
> a third doped region within said substrate having opposite dopant type from said substrate which when taken with said second doped region within said first doped region forms a doped pair;
>
> a conductor element from said second doped region to a first voltage source; and
>
> a conductor element from said third doped region to a second voltage source;
>
> ***wherein the first doped region is substantially free of doped regions having the same dopant type.***

(*Emphasis Added*).

Applicant respectfully asserts that each of *Lee* '414, *Watanabe* and *Ito* is legally deficient for the purpose of anticipating claim 16. Specifically, Applicant respectfully asserts that none of these references teaches or otherwise discloses at least the features/limitations emphasized above in claim 16.

With respect to *Lee* '414, that reference does not teach or suggest "wherein the first doped region is substantially free of doped regions having the same dopant type." This unique feature is to provide a base collector junction in addition to the protection diode junctions, which reduces the leakage characteristic of a single diode junction as in prior art. See lines 9-14 of page 5 and lines 12-15 of page 8 of present application. Additionally, *Lee* '414 does not teach or

suggest "only one second doped region within said first doped region having opposite dopant type to said first doped region."

Conversely, *Lee* '414 provides a displacement current trigger SCR, wherein a first n^+ contract region 13 is formed in n-well 12. See figure 4 and column 4 lines 43-44 of *Lee* '414. Therefore, Applicant respectfully asserts that the rejection of claim 16 under *Lee* '414 is improper and requests that the rejection be removed.

With respect to *Watanabe*, that reference does not teach or suggest "wherein the first doped region is substantially free of doped regions having the same dopant type." In particular, *Watanabe* provides a MIS field effect transistor, wherein an anode region 4 of the same conductivity as that of the substrate 1 is formed in the N-type region3 and another anode region 5 similar to the first anode 4 in impurity concentration is formed at the periphery of the region 3. See figure 2 and column 2 lines 15-25 of *Watanabe*. Therefore, Applicant respectfully asserts that the rejection of claim 16 under *Watanabe* is improper and requests that the rejection be removed.

With respect to *Ito*, that reference does not teach or suggest "wherein the first doped region is substantially free of doped regions having the same dopant type." In particular, *Ito* provides a semiconductor protection circuit, wherein a N-type high impurity concentration layer 24 is formed in the surface of the N-type well layer 14 for connection of the N-type well layer 14. See figures 6-9 and column 6 lines 15-31 of *Ito*. Moreover, *Ito* does not teach or suggest "only one second doped region within said first doped region having opposite dopant type to said first doped region." Specifically, *Ito* teaches forming P-type drain and source layers 20 and 21 in the surface of the N-type well layer 14. See figures 6-9 and column 6 lines 10-14 of *Ito*. Therefore, Applicant respectfully asserts that the rejection of claim 16 under *Ito* is improper and requests that the rejection be removed.

Since claims 17 - 24 are dependent claims that incorporate the limitations of claim 16, and are not otherwise rejected in the Office Action, Applicant respectfully asserts that claims 16 - 24 are in condition for allowance. Additionally, claims 17 – 24 recite other limitations that can serve as an independent basis for patentability.

Rejections under 35 U.S.C. 103

The Office Action indicates that claims 2 and 3 are rejected under 35 U.S.C. §103 as being unpatentable over *Lee* '999 in view of *Borland* (U.S. Patent. 5,814,866). Additionally, the Office Action indicates that claims 4 and 5 are rejected under 35 U.S.C. §103 as being unpatentable over *Lee* '999 in view of *Curry* (U.S. Patent. 5,761,697). Applicant respectfully traverses the rejections.

In particular, Applicant respectfully asserts that the cited combinations are legally deficient for the purpose of rendering the rejected claims obvious, because the combination does not teach or reasonably suggest at least the features/limitations described above as lacking in Lee '999. Therefore, Applicant respectfully asserts that the rejection of claim 2 - 5 is improper and requests that the rejection be removed.

Newly Added Claim

Upon entry of the amendments in this response, Applicant has added claim 34. Applicant respectfully asserts that claim 34 is in condition for allowance for at least the reason that this claim is a dependent claim that incorporates the features/limitations of claim 1, the allowability of which is described above.

Cited Art of Record

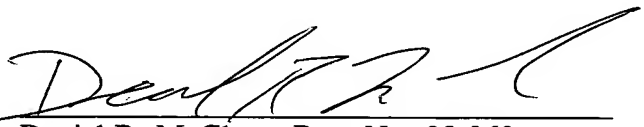
The cited art of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this Amendment and Response. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

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